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An Ultra Low Power Successive Approximation ADC for Wireless Sensor Network

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Abstract
In this paper, a new low-power SARADC is presented. In the presented design, the frequency dependency of the power rather than the conventional supply voltage is emphasized. Our evaluations show that when the frequency of a mixed signal system drops down, the ratio of power consumption in analog and digital units have different patterns. In this respect, for our target study of SARADC the power share in analog is about constant while the share of digital sections is rapidly reduced. This means that to lower the total power, the analog section must be optimized. In our target study, the SARADC has a major analog unit as a comparator. The frequency of the target design is selected in range 50 KHz - 200 KHz, which is the conventional range of operations for ADC in Wireless Sensor Network (WSN) nodes. The 6bit SARADC reported here consumes only 4.96 µW at 100 KHz. Ultra low power consumption of our ADC makes this suitable for WSN node applications. The proposed 6bit SARADC is designed and simulated in 90nm CMOS at 1v supply voltage.

Keywords: Capacitor Array, Low Power Design, Mixed Signal Design, SARADC

INTRODUCTION

Nowadays, more and more applications are built with very stringent requirements on power consumption. The power consumption is becoming one of the most critical factors for electronic systems, such as wireless systems. The need for the development of low power and low voltage circuit techniques and system building blocks has been increased by high importance of the energy consumption [1].

In the mixed-signal design, both parts of analog and digital must be modeled and simulated together. The rate of power consumption and proper functionality in analog and digital sections are different. The mutual effects of analog and digital sections are also remarkable. Successive Approximation Analog to Digital Converter (SARADC) is a mixed-signal design. The Wireless Sensor Network (WSN) node is a good sample of mixed signal design.

Digital converters are vital and widely used in mixed signal design and implementation. Analog to Digital Converter (ADC) samples the input analog signal and outputs digitalized bit equivalent.

Power profile is a global view of the power consumption in sub-units of a target system. This schema is useful with equal validity in both of analog and digital sections. This means that for proposed target mixed-signal design like WSN node power profile is useful.

Power profile enables to have more efficient design. Evaluation results show that, the comparator is a major unit in the SARADC and consumes most of the total power. Therefore, having low power comparator results in a low-power SARADC.

One of the best known low power SARADC for WSN applications is presented in [2]. In this structure they have implemented a low-power design by utilizing the sleep mode on major units of the design. In the sleep mode the unused blocks are powered off during the main operation. They proposed two different designs of 8-bit and 12-bit with two different sampling rates of 100Ks/s and 200ks/s. Their design consumes about 25µw power at 12-bit operating mode. Proposed SARADC is not as complex as of [2]; optimized comparator in the proposed SARADC comes with a simpler structure while in the same frequency range of [2] operates in lower power.

In [3] one ultra-low power 8-bit SARADC with only 3.1µW power is introduced. In [3] one ultra-low power comparator is designed and used. Unfortunately, the proposed comparator in [3] is not working properly for lower voltages, and it does not result in rail-to-rail design.

In the presented design, a 6-bit SARADC with 90nm CMOS technology at 1v supply voltage with Hspice is designed and simulated. The proposed design is best suitable for WSN applications. This paper is organized as follows: WSN node is briefly described in second section. SAR architecture and circuits are introduced in section three. Power profile and low power comparator design are explained in forth section. The measured results are described in section five, and finally the conclusion is expressed in section six.

WSN Node

Power issue is the most important problem in WSN node design. If the power source delivery to WSN node is not durable like photo cells and thermal energy, then the life time of the node is equal to the life time of the battery. Therefore, the lower the power in WSN node, the more the life of the node [4, 5].

The basic building blocks for a conventional WSN node are depicted in Fig. 1. In each node at least there is one ADC. In WSN applications and due to the IEEE 802.15.4 the frequency rate of operating conditions is usually between 50KHZ and 200KHZ. The best choice of ADC for WSN applications is Successive Approximation ADC SARADC). SARADC comes with benefits of low-bit rate suitable for WSN applications and is a good candidate for WSN nodes.

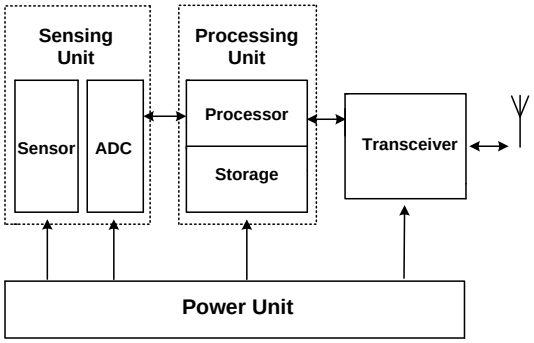

Figure 1. building blocks for a conventional WSN node[6].

SAR ADC Architecture

There are different topologies for SARADC. In proposed design, the SARADC shown in Fig. 2 is used for basic unit. This unit comes with a single comparator that is suitable for low power design. In this design, the number of bits and resolution is not related to the number of used comparators and in turn gains to have more focus on the low power with emphasis on a single comparator. In this design, a simple array of capacitors and switches is used for binary search algorithm. The capacitor array is used for Digital to Analog Converter (DAC) unit. Since the target design is six bits, which need seven capacitors, one capacitor for each bit and one extra capacitor for correction of the division operator in each switching step. Due to the SARADC structure, for six bits It need eight clock steps, one step for initialization, one for output reset or flush and six steps for 6 individual output bits. The capacitor array is used for Digital to Analog Converter (DAC) unit.

Since the target design is 6 bits, which need seven capacitors, one capacitor for each bit and one extra capacitor for correction of the division operator in each switching step. Due to the SARADC structure, for six bits eight clock steps, is needed; one step for initialization, one for output reset or flush and six steps for six individual output bits. One major drawback in SARADC is the need for two reference voltages for charge and discharge of capacitor arrays. The need to have two different supply voltages in the single chip may result in extra power consumption on the die even when the converter is in the sleep mode. In order to avoid two reference voltage instances, two voltages of 0 and V_{DD} are selected. In this case, the comparator is working with Vref=V_{DD}.

The selection of V_{DD}=Vref comes with a major drawback. In this case, the power supply rejection ratio is poor and the variations on V_{DD} or Vref directly applied on the output bits [3].

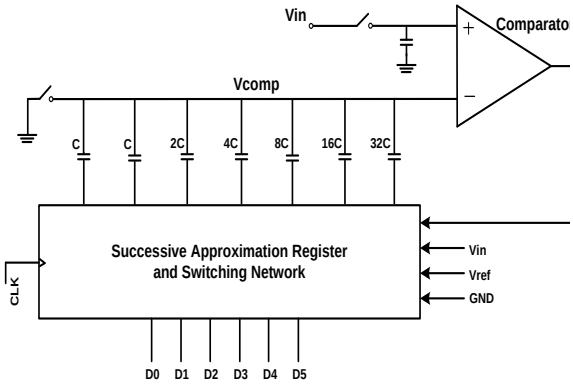

Figure 2. Structure of Successive approximation ADC.

Comparator

In the WSN applications with sampling rates of (50Ks/s – 200 Ks/s) the rule of comparator is more critical. In a WSN node more than 70% of the total power of SARADC is used in comparator. This means that in the low power targeting for SARADC, comparator is the suitable block for emphasis.

The schematic of an ultra low power comparator is illustrated in Fig. 3, this structure is used in [4, 5]. The shown structure is very low power. In this comparator, there is a one pair of NMOS at the input. This pair is not working properly in the low voltages (near zero). Therefore, the comparator is not working properly in the sub threshold region of [0-Vth].The comparator of Fig. 3 works very fine for the voltage range of [Vth -Vdd]. In this region the comparator works with a very low power. The PMOS input pair for the comparator in turn is not working properly in the near V_{DD} rang of [Vdd-Vth, Vdd].

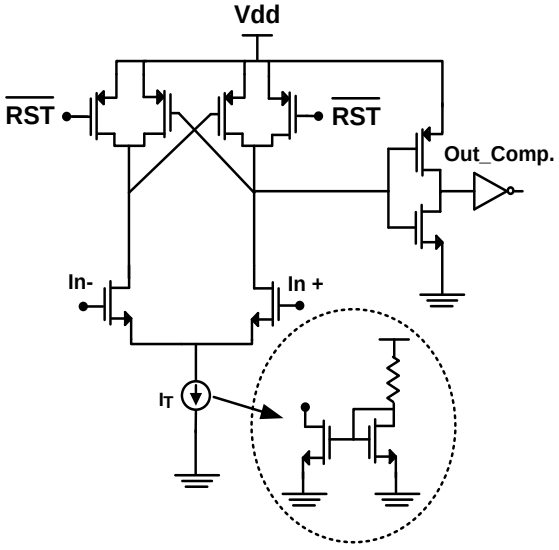

Figure 3. Ultra low power comparator circuit schematic[3].

Optimized Comparator

The idea of combining NMOS and PMOS pair at inputs is first introduced in [7]. Based on the presented idea in [7] the combined input pair of PMOS and NMOS for input of Fig. 3 is applied. The proposed comparator is resulted that shown in Fig. 4. Optimize comparator not only overcomes the rail-to-rail swing problem but also results in a very low power design.

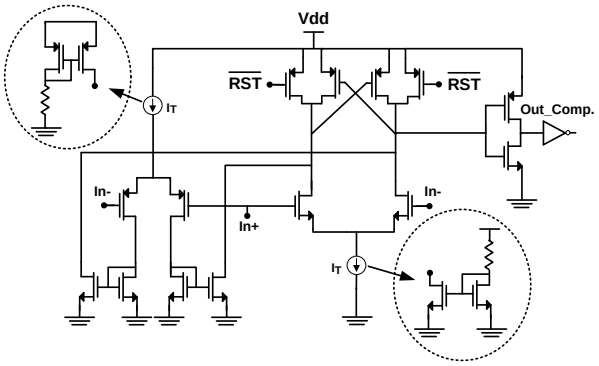

Figure 4. Optimized comparator circuit schematic.

Capacitor Array and switching network

The capacitor array has two main functional tasks in SARADC, first is the sampling of the input signals, and second conversion of digital outputs into analog input for comparison.

In Fig. 5 a conventional capacitor array structure based on [8] is shown. It is seen that in this topology, the input voltage is directly connected to the capacitor array, and switches are switching between input voltage and two values of GND and V_{DD}.

In the structure of Fig. 6 that used in this work the input is directly connected to positive voltage via a switch.

In this structure capacitor, C_0 is used for correction of the divide by two and since it is always connected to earth, there is no need a switch for it. The used switches in the design only toggle between two DC voltages of Vref = V_{DD} and GND and there is no need for input signal sampling in that switches. This means that there is no need for optimization on switches and single transistor switches applicable in this design.

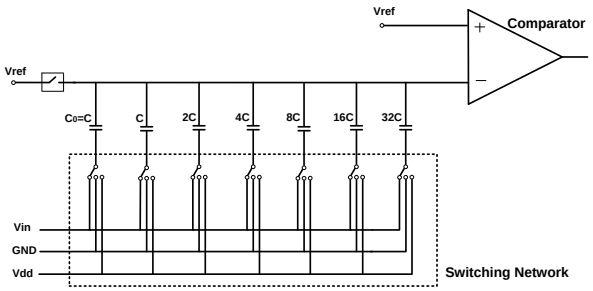

Figure 5. Conventional capacitor array structure [8].

The other switch is used for reset and is connected to negative input of the comparator. This switch is implemented by a simple transistor too. It is seen that the most important switch in this topology is the switch connected to positive input of comparator. It is the basic sampling switch.

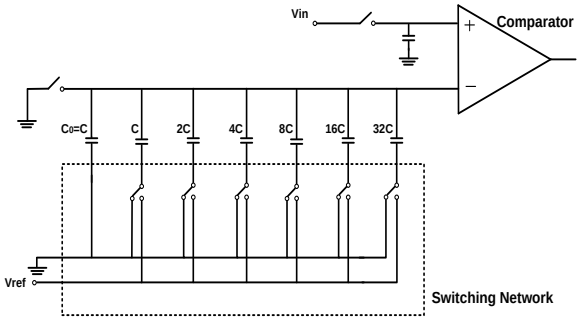

Figure 6. Structure of the proposed capacitor array.

Power And Power Profile

The ADC converter contains some building blocks. Each block has its own share in the total power consumption. The spliced power share in our proposed SARADC working at 100 KHz is summarized in table 1. It is seen that the total power is below 5µW.The power profile of our proposed SARADC is depicted in Fig. 7. The power profile versus frequency of the proposed SARADC for the frequency range of [100 KHz-20MHz] in log. scale is illustrated in Fig. 8 that confirms our results.

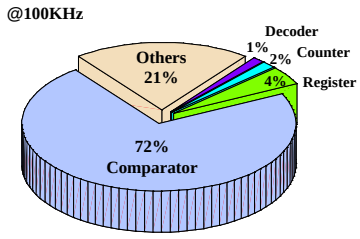

Figure 7. The power profile of our proposed SARADC.

To show the correct operation of the proposed low-power SARADC, a sample simulation is illustrated in Fig. 9. As seen in Fig. 9, a sin input at the frequency of 20 KHz is applied and sampled with 100 KHz. The blue waveform is the output of the sampler. The green signal is the applied clock, and the orange signal is the output of 6 bit comparator.

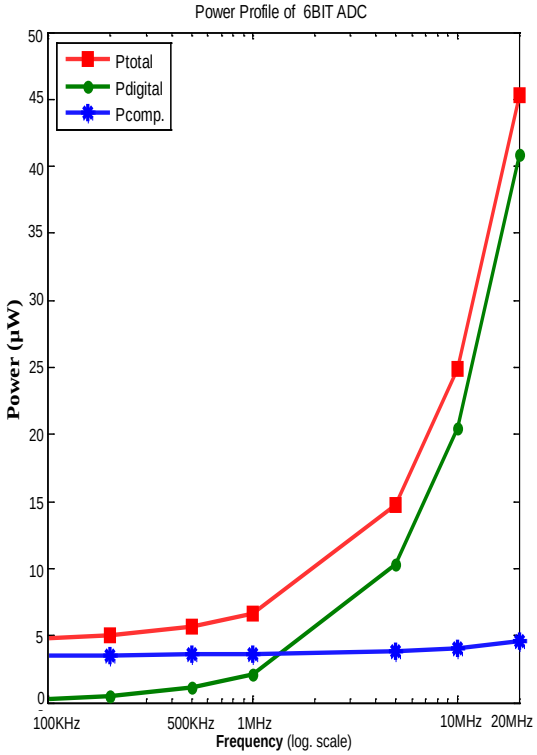

Figure 8. Power profile for optimized SARADC with spliced share of Analog and Digital sub-sections in log. scale.

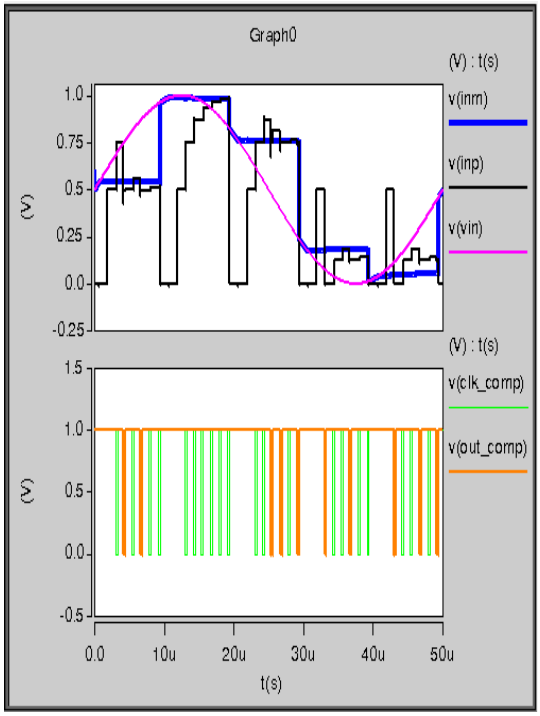

Figure 9. The 20KHz input sin wave, output of S/H circuit and comparator output sample simulation results.

MEASURED RESULTS

To show the effectiveness of our proposed SARADC, the typical calculations on it are presented in this section.

Measured Results

In Fig. 10 a typical 1024 points FFT of the output spectrum in the input frequency of 1.5625 KHz with 1v supply is depicted. The ENOB of the proposed SARADC is ENOB = 5.87.

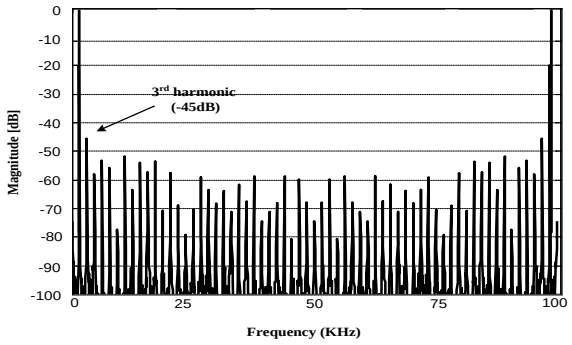

Figure 10. Typical FFT for input freq. of 1.5625 KHz and 1v.

FOM Calculation

FOM is calculated with equation (1).

$$FOM = \frac{power}{2 \times BW \times 2^{ENOB}} \quad (1)$$

Hence for Average Power = 4.97µW and ENOB=5.87 with input frequency of 1.5625 KHz, FOM is 849 fj per Conversion step. The overall performance list of the proposed SARADC is shown in Table 2. and Table 3, summary of comparison of our designed SARADC versus four other related designs is presented.

Table 1. Average power of SARADC sub-blocks

Parts	Average power At 100KHz
Comparator	3.557µW
Registers	220.894nw
Counter	81.718nw
Decoder	67.123nw
Others (switches, capacitor Array)	1.03µW
Entire ADC	4.961µW
Comparator	3.557µW

Table 2. Comparison of the proposed SARADC with another SARADCs.

sources	[5]a	[5]b	[6]	[7]	[8]	[1]	This work
Technology (CMOS)	0.18µm	0.18µm	0.25µm	0.18µm	0.25µm	90nm	90nm
Resolution	8bit	8 bit	8 bit	12 bit	6 bit	8 bit	6 bit
Supply Voltage	1v	0.9v	1v	1v	2.5v	1.2v	1v
Sampling Rate(S/s)	400k	200k	100k	100k	1M	1.4k	100k
ENOB (bit)	7.31	7.58	7.9	10.55	5.53	7.8	5.9
Power Dissipation	6.15µw	2.47µw	3.1µw	25µw	1.19mw	13.4 µw	4.97µw
FOM (fj/step)	97	65	-	167	1288	-	849

Table 3. Overall Specs of the Proposed Low-Power SARADC .

Specs	Measured
Technology	90nm CMOS
Voltage Supply	1V
Input Range	Rail- to – Rail
Sampling Rate	100KHz
ENOB(at:1.5625KHz)	5.876bit
Power Dissipation	4.97 µw
FOM	0.849 /step

CONCLUSION

A 6 bits SARADC with 100 Ks/s at V_{DD} = 1V is designed for WSN applications. A power profile for frequency of mixed signal WSN node design is studied and the impacts of analog and digital sub sections are studied. Results show that the impact of analog section in the lower range of frequencies is more than digital section. We focused on analog section and designed a low-power comparator. The total power of the proposed SARADC is about 4.97 µW at 100 KHz.

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