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A New High Speed, Area Efficient 7-2 Compressor for Fast Arithmetic Operations

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Abstract
This paper presents a new high speed, low power 7-2 compressor which is constructed according to a sensible combination of pass transistor logics and static logics. It is constructed of a new 5-4 arithmetic block and two 3-2 counters. The new 5-4 arithmetic block is designed based on a new truth table. So, a simple 7-2 compressor is designed only with 124 transistors. Therefore, a decrease of gate level delays is achieved which lowers its power dissipation. Also, the driving problems are decreased, considerably. Furthermore, the decrease of middle stages' capacitances and utilizing voltage full swing logics have enhanced the speed of cascaded operations. The total latency and power dissipation of the proposed 7-2 compressor are about 470ps and 670μw, respectively, which is simulated by HSPICE using TSMC 0.18μm CMOS technology.

Key words: 7-2 Compressor; High speed; Area Efficient; Pass transistor logic; 5-4 arithmetic block

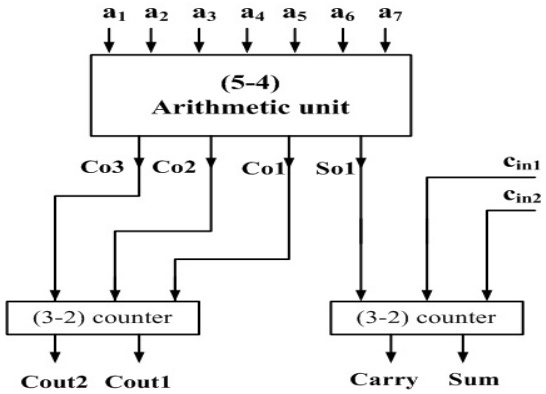
INTRODUCTION

As the demand for higher performance arithmetic units such as high speed multipliers, efforts have been focused on performing new algorithms and improving func- tionality of their constitutive elements. Compressors are one of the critical components of multiplier circuits that are being widely utilized in high speed systems such as digital image processing. Multiplication is basically a two-step process, consisting of formation of partial pro-ducts followed by the accumulation stage. To enhance the speed of partial product's formation stage, many methods have been utilized such as booth encoding method which reduces the number of partial products generated [1-4]. However, in multiplication higher than 16 bits, the most significant delay belongs to the summation stage. A high performance method to lower the latency of the accumulation stage is to use carry save adders (CSA) in Wallace and Dadda trees[5]. A major intention of carry save adder arrangements is obtained by utilizing compressor structures such as 7-2 compressors.

Many methods are utilized to implement 7-2 compressors [6-11]. Conventional structure of a 7-2 compressor is depicted in Fig.1. (a). It is made up of five full adders and have the delay of 4 full adders [7-8]. All of 7-2 compressors are abided by:

$$a_1 + a_2 + a_3 + a_4 + a_5 + a_6 + a_7 + C_{in1} + C_{in2} = Sum + 2 \cdot (Carry + C_{out1}) + 4.(C_{out2}) \quad (1)$$

Based on Eq. (1), 7-2 compressors of [8],[10-11] are designed. Also, 7-2 compressors can be constructed by threshold logics (TL), Hybrid Threshold-Boolean logics (HTBL) [9] and three-level MOS current-mode Logic (MCML) gates [6].



(b)

Fig.1 (a) Conventional architecture of a 7-2 compressor. (b) Proposed structure of a 7-2 compressor.

As depicted in Fig.1. (b), our proposed structure is constructed based on a new 5-4 arithmetic unit and two 3-2 counters. Utilizing a sensible combination of static and pass transistor logic gates with voltage full swing features have decreased the middle stages' capacitances and have increased the speed of cascaded operations. So, this design is achieved to a lower latency over previous works. Also, based on the new arithmetic unit, this design is achieved to an area-efficient architecture and it is constructed of only 124 transistors.

The rest of this paper is organized as follows: Our proposed structure is presented in Sec.2. Sec.3 offers the proposed 7-2 compressor's results by a comparison with previous works. Finally, Sec.4 includes the concluding remarks.

STRUCTURE

Constitutive elements

In this part, we concentrate on some arithmetic units and their hierarchies. As depicted in Fig.2. (a), a XOR-XNOR circuit is introduced to be utilized in our proposed design, generating XOR and XNOR outputs simultaneously [12]. Besides, this module would eliminate the weak logic problem due to a pair of feedback PMOS-NMOS transistors. The overall latency of this circuit is assumed to be equivalent with one gate level delay. The other unit that is utilized in this article, is a (2-1) multiplexer. As depicted in Fig.2 (b), it is constructed of two transmission gates (TGs) and a select control signal by its complementary form. So full swing output will be achieved. Also due to the reduction of input gate capacitances, the overall latency of this block is decreased [13].

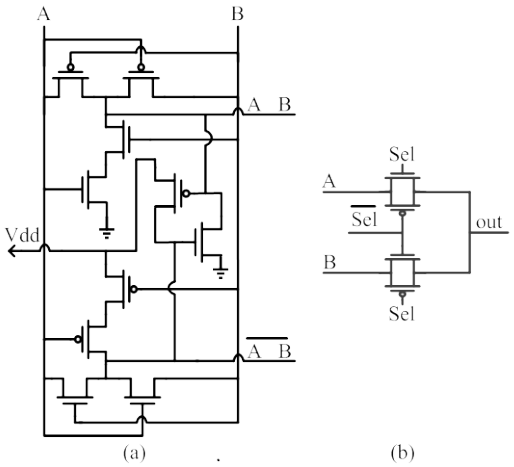


Fig.2. (a) XOR-XNOR block (b) (2-1) multiplexer

Proposed new 7-2 compressor

A 7-2 compressor gets a_1, a_2, a_3, a_4, a_5, a_6, a_7 inputs with weights of one and generates two outputs Sum and Carry with weights of one and two, respectively. Also, it gets two input carry bits C_{in1}, C_{in2} with the same weight of inputs and generates two output carry bits, C_{out1}, C_{out2} with weights of two and four, respectively. As depicted in Fig.1. (b), our proposed design is constructed of a 5-4 arithmetic unit and two 3-2 counters.

New 5-4 arithmetic unit

The new 5-4 arithmetic unit gets seven inputs and generates four outputs as the following equations with the weights of one, two, two and two, respectively:

$$S_{o1} = a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7 \quad (2)$$

$$C_{o1} = ((a_1 \oplus a_2 \oplus a_3) \oplus (a_4 \oplus a_5 \oplus a_6)) \cdot a_7 + \overline{((a_1 \oplus a_2 \oplus a_3) \oplus (a_4 \oplus a_5 \oplus a_6))} \cdot (a_1 \oplus a_2 \oplus a_3) \quad (3)$$

$$C_{o2} = (a_1 \oplus a_2) \cdot a_3 + \overline{(a_1 \oplus a_2)} \cdot a_1 \quad (4)$$

$$C_{o3} = (a_4 \oplus a_5) \cdot a_6 + \overline{(a_4 \oplus a_5)} \cdot a_4 \quad (5)$$

Table1. New truth table used to implement new 5-4 arithmetic unit

Y	Z	X	So_1	Co_1
0	0	0	a_1	a_7
0	0	1	$\overline{a_1}$	a_7
0	1	0	$\overline{a_1}$	a_1
0	1	1	a_1	$\overline{a_1}$
1	0	0	$\overline{a_1}$	a_1
1	0	1	a_1	$\overline{a_1}$
1	1	0	a_1	a_7
1	1	1	$\overline{a_1}$	a_7

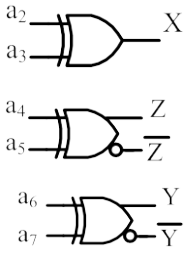


Fig.3. Implementations of control signals X, Z and Y.

So_1 and Co_1 outputs are the main factors that determine the latency of the new (5-4) arithmetic unit. So, decreasing this delay depends on shortening these outputs' critical paths. According to the equations (2) and (3), and based on control signals X, Z and Y, the new proposed truth table is achieved as Table.1 for generating So_1 and Co_1 outputs. As depicted in Fig. 3, control signals X, Y and Z by their complementary outputs are generated simultaneously to be utilized in the proposed design as $X = a_2 \oplus a_3$, $Z = a_4 \oplus a_5$ and $Y = c_{in1} \oplus c_{in2}$.

As depicted in Fig.4. (a), based on Table.1, a XOR-XNOR circuit is utilized to generate E and F signals as the following equations:

$$E = (X \cdot a_1) + (\overline{X} \cdot \overline{a_1}) \quad (6)$$

$$F = (X \cdot \overline{a_1}) + (\overline{X} \cdot a_1) \quad (7)$$

As shown in Table 1, the $\overline{So_1}$ output is equivalent with *F* for *Z*=0 and *Y*=1 or *Z*=1 and *Y*=0. Also it is equivalent with *E* for *Z*=*Y*=0 or *Z*=*Y*=1. So, it is obtained based on different values of control signals *Z* and *Y* and signals *E* and *F* as the following equation, shown in Fig.4. (b):

$$\overline{So_1} = (Y \oplus Z) \cdot F + \overline{(Y \oplus Z)} \cdot E \quad (8)$$

Also, according to Table 1, the $\overline{Co_1}$ output is equal to *E* for different values of *Z* and *Y*. Also it is equivalent with $\overline{a_7}$ for *Z*=*Y*=0 or *Z*=*Y*=1. The following equation shows the $\overline{Co_1}$ output generation, shown in Fig.4. (c) :

$$\overline{Co_1} = (Y \oplus Z) \cdot E + \overline{(Y \oplus Z)} \cdot \overline{a_7} \quad (9)$$

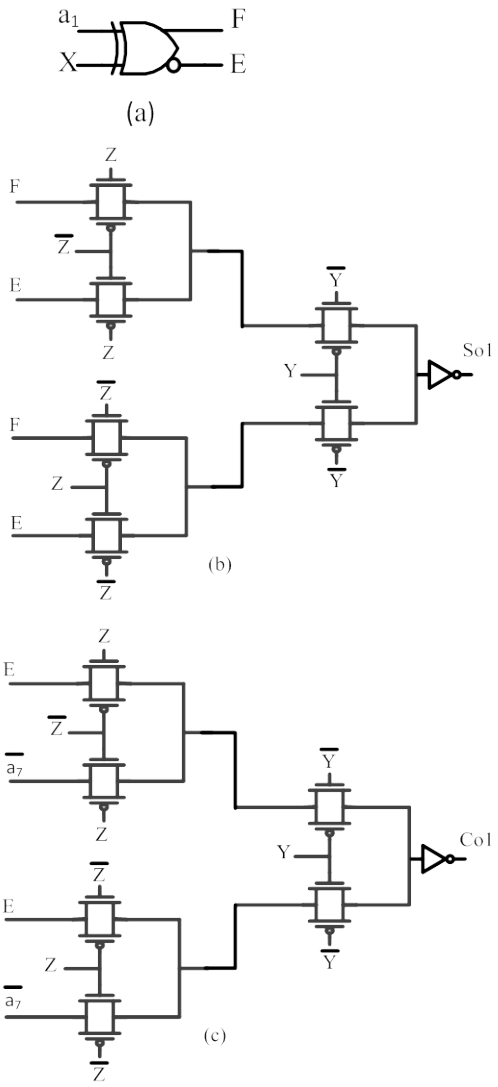


Fig.4 (a) Implementation of signals E and F. (b) Implementation of the So1 output. (c) Implementation of the Co1 output.

As depicted in Fig.4.(b) and Fig.4 .(c), So_1 and Co_1 outputs are achieved after one inverter to avoid from driving problems.

It should be noted that when the gate channel of a TG is ready to transmit its input to the output before receiving any inputs, its latency is decreased considerably. As depicted in Fig.4, Z and Y signals are generated one gate level delay earlier than E and F signals. So, the channels of TGs are ready to transmit their input signals to outputs and so on, the latency is decreased considerably. As a result, So_1 and Co_1 outputs are generated after 2 gate level delays and plus 2 ready-channel transistors.

The outputs C_{o2} and C_{o3} of the new 5-4 arithmetic unit are generated according to the following rewritten equations of (4) and (5):

$$C_{o2} = a_1 \cdot a_2 + a_3.(a_1 + a_2) \quad (10)$$

$$C_{o3} = a_4 \cdot a_5 + a_6.(a_4 + a_5) \quad (11)$$

Fig.5.(a) and Fig.5.(b) depict the implementations of C_{o2} and C_{o3} outputs. The advantage with these circuits is their full voltage swings at the output nodes and buffered output signals. Also, they decrease the driving problems in further stages, considerably. As shown in Fig.5, C_{o2} and C_{o3} outputs are generated after one gate level delay.

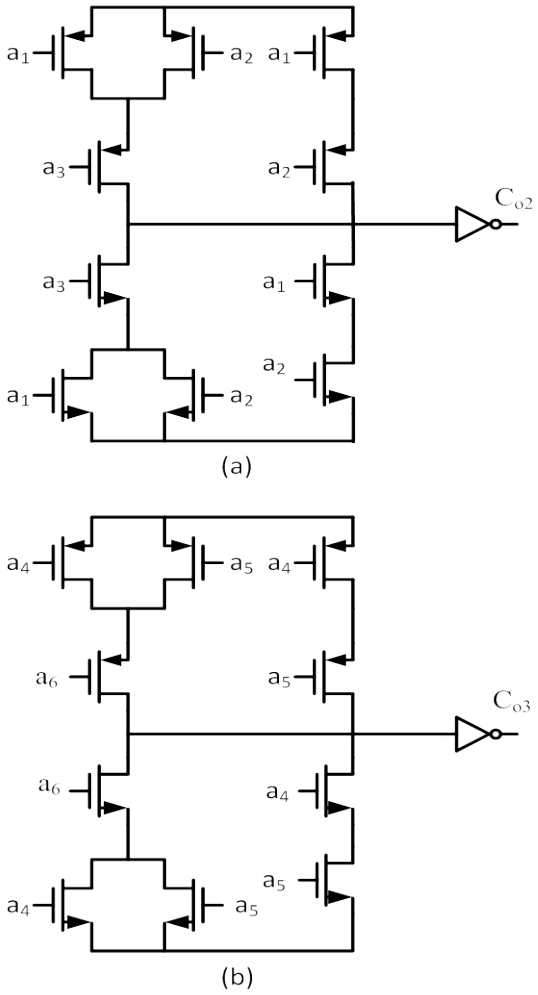


Fig.5. (a) Implementation of C_{o2} (b) Implementation of C_{o3}

Final arrangements

As depicted in Fig.6, a18-transistor 3-2 counter is utilized. Due to the use of mentioned XOR-XNOR block of Fig.2.(a), the threshold problem in internal nodes is removed. Also, it employs a XOR circuit instead of an inverter [14] to remove the possible short circuit power consumption.

As depicted in Fig.6 (a), the inputs of XOR-XNOR block are Co_2 and Co_3. So, the Carry outputs of proposed 7-2 compressor are achieved independently from carry input bits, as the following equations:

$$C_{out1} = Sum(C_{o1}, C_{o2}, C_{o3}) \quad (12)$$

$$C_{out2} = Carry(C_{o1}, C_{o2}, C_{o3}) \quad (13)$$

So, carry output bits are achieved after 2 gate level delays and 1 TG plus 2 ready -channel transistors.

As depicted in Fig.6. (b), Sum and Carry outputs are generated based on carry output bits of the previous 7-2 compressor and So_1 output as the following equations:

$$Sum = Sum(C_{in1}, C_{in2}, S_{o1}) \quad (14)$$

$$Carry = Carry(C_{in1}, C_{in2}, S_{o1}) \quad (15)$$

So, the latency of critical path in our proposed structure includes 3 gate level delays and 2 TGs plus 2 ready-channel transistors.

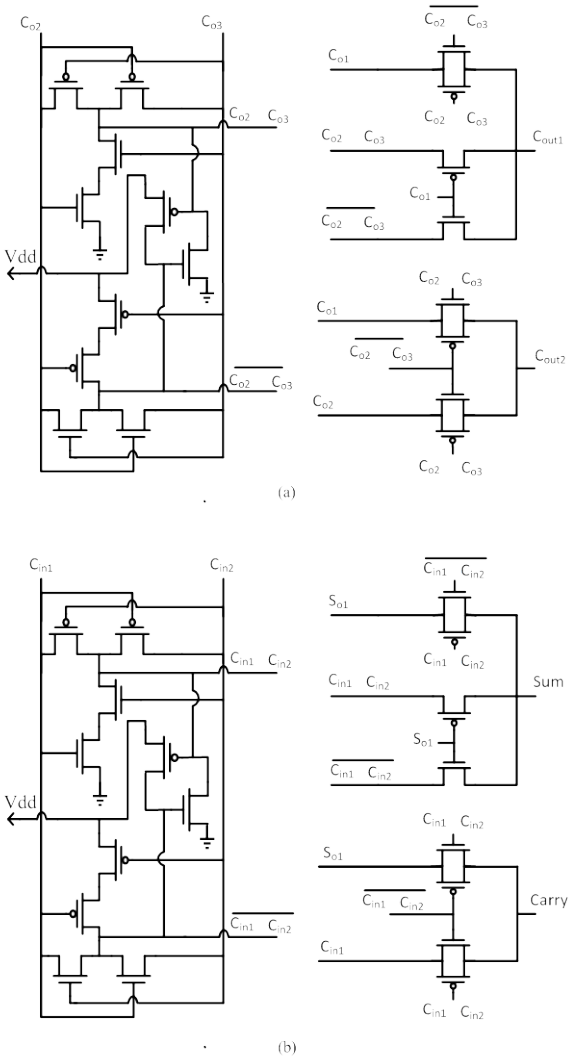


Fig.6. (a) Implementation of C_{out1} and C_{out2} (b) Implementation of Sum and Carry

COMPARISON AND SIMULATION RESULTS

The overall latency of our proposed 7-2 compressor includes 3 gate level delays and 2 TGs plus 2 ready-channel transistors in its critical path which confirms the superiority of our proposed design over prior works [6-11]. Since the output voltage of logics in this architecture keep full swing voltages, so it leads to a fast switching operation. Also, driving problems are decreased considerably by use of logic gates with no threshold problems, inverters after So_1 and Co_1 outputs and a XOR-XNOR gate for E and F signals' generation. Therefore, only two transmission gates (TGs) remain cascaded. If each four TGs is considered as one multiplexer cell (according to the pass transistor logics) the total gate count of our work reaches to 14 logic gates. Also, the sizes of NMOS and PMOS transistors of TGs are considered the same, while initial TGs are considered a little greater in size to avoid driving problems. Based on new arithmetic unit, the proposed architecture is reached to an area-efficiency and is constructed of only 124 transistors.

Post layout simulations are performed based on TSMC 0.18 μm CMOS technology and 1.8 supply voltage by HSPICE. Layout of proposed work is illustrated in Fig.7 which consumes a small active area at the size of 58.33 μm × 38.21 μm. All measurements are considered at a frequency of 250MHz. The simulation environment is shown in Fig.8. Each input is driven by buffered signals and each output is loaded with buffers. As shown in Fig.8, the compressors are running in parallel and the left-side compressor is considered to obtain the simulation results, as an actual simulation environment. For the propagation delay, we have taken the time from input signal reaching 50% to the output signal reaching 50% of the supply voltage. Also, the average power consumption of left-side compressor is considered, by excluding the power consumption of the buffers. The overall latency and the average power consumption are obtained as 470ps and 670μw, respectively. Table II includes comparison results between our design and previous works.

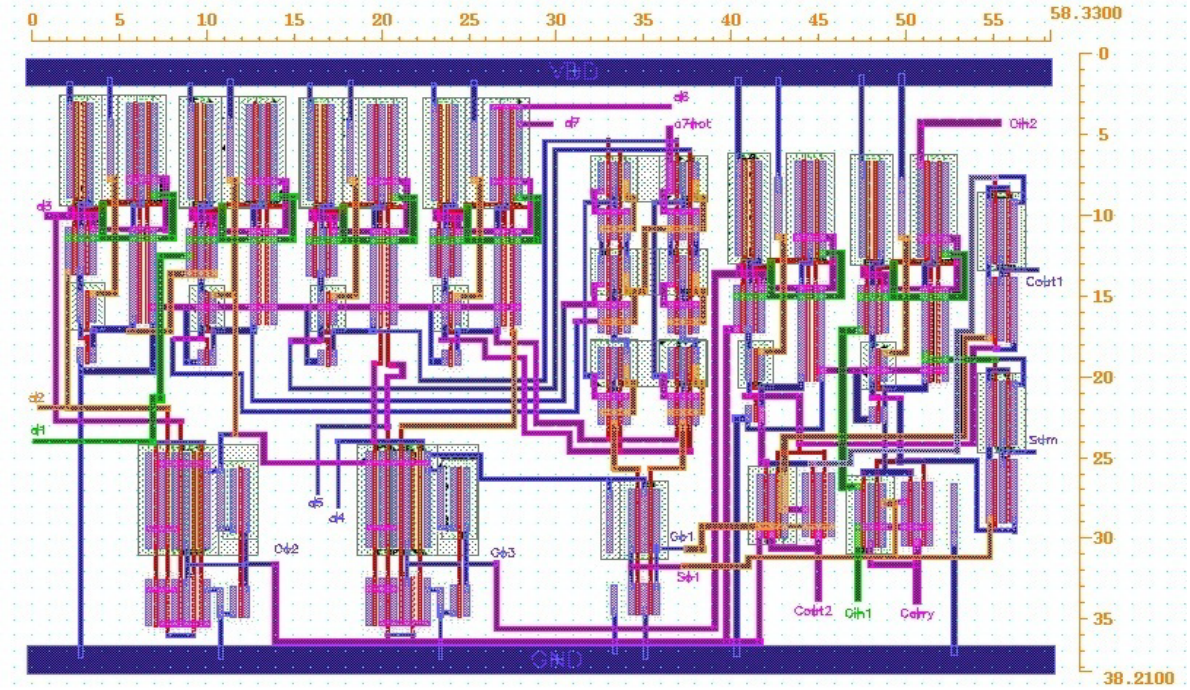


Fig.7. Layout of proposed 7-2 compressor

Table 2. Comparison of proposed 7-2 compressor with previous works

Work	Techn-ology	Gate level delays	Gate Count	# of Tran	Delay (ps)	Power (µw)
[6]	0.18 µm	4 three-level MCML gates	10 MCML	120	493.57	995.05
[7]	0.25 µm	4.16 full- adder cell	-	170	1250	-
[9] (TL)	0.25 µm	2.12 full- adder cell	-	415	638	-
[9] (HTBL)	0.25 µm	1.63 full- adder cell	-	285	489	-
[10]	0.18 µm	6 gates	15	141	610.16	1496.6
[11]	0.18 µm	3 gates + 6 Nand gates	>31	166	1000	-
Proposed	0.18 µm	3gates+ 2TGs + 2 ready-channel transistors	14	124	470	670

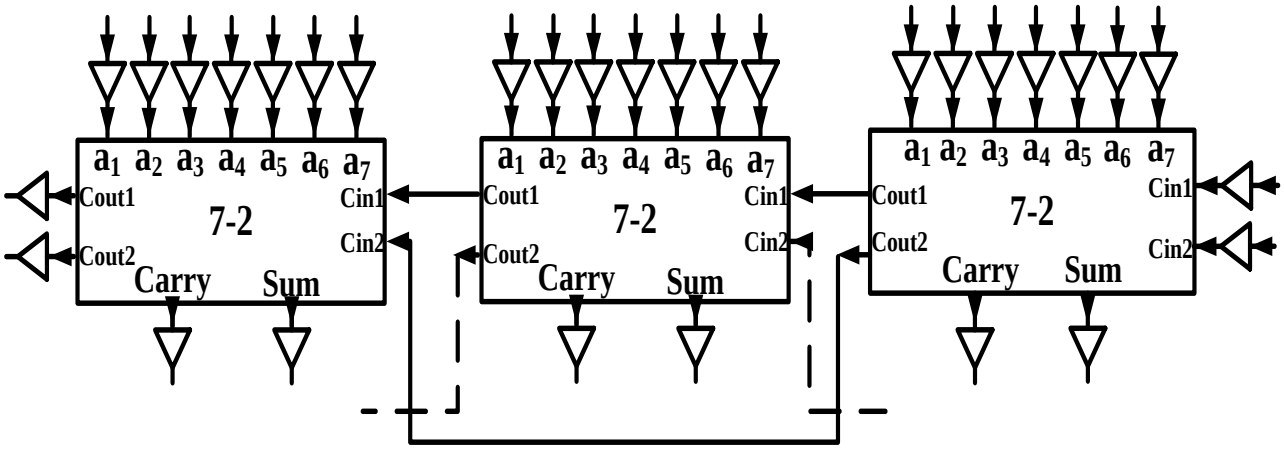


Fig.8. 7-2 compressor simulation environment

The results of [6] and [10] are extracted from [6] that are tested by 0.18 μm CMOS technology by 1.8V supply voltage. Also, proposed design of [11] is tested by 1.8V supply voltage. The results of [7] and [9] are extracted from [9] which is simulated by 0.25 μm CMOS technology with 2.5V supply voltage.

CONCLUSION

In this article, a new 7-2 compressor is developed to be utilized in high speed systems. This architecture is constructed based on a newly designed truth table and based on a sensible combination of pass transistor and static logics. Due to the simple structure and also reduced capacitances of middle stages, the overall delay of proposed design and its power dissipation are decreased. Also utilizing logic circuits with full swing voltages enhances the speed of cascaded operations. According to the critical path of proposed structure, it includes 3 gate level delays and 2 TGs plus 2 ready-channel transistors in its critical path. Utilizing only 14 gates including 124 transistors to implement this circuit admits the proposed design's great area-efficiency in comparison with previous works.

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